Single-Event Effects Induced on Atom Switch-based Field-Programmable Gate Array

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***Abstract*—Single-event effects (SEEs) of atom switches (ASs) embedded on 40-nm complementary metal–oxide–semiconductor (CMOS) are investigated with both heavy-ion and pulsed laser irradiation. In the evaluation of an AS-based field-programmable gate array (AS-FPGA), ASs show immunity against the irradiation and there is no change of the state of ASs both in a crossbar switch and memory in lookup tables (LUTs). ASs are not supposed to make any single-event transient (SET) noise when the ions hit. However, the CMOS layer shows SETs, and new approaches are proposed to solve the SET in CMOS, especially for AS-FPGA application.**

***Index Terms*—Atom switch (AS), heavy ions, pulsed laser, single-event effects (SEEs), single-event transient (SET).**

I. Introduction

FIELD-PROGRAMMABLE gate arrays (FPGAs) are becoming widely used in space applications along with the growing demand for high-throughput satellites. The unique programmable feature of FPGAs enables not only various functional capabilities but also a short development turnaround time and low cost, as compared with manufacturing application-specific integrated circuits. There are currently three types of FPGAs available in the space industry market: antifuse-based, static random access memory (SRAM)-based, and flash-based FPGAs. While the antifuse-based FPGA is physically programmed once with the desired circuits on it, both SRAM-based and flash-based FPGAs have the reprogrammable capability. However, these SRAM- and flash-based FPGAs suffer from leakage power loss with the latest semiconductor manufacturing processes and are also vulnerable to single-event effects (SEEs) [1].

The atom switch FPGA (AS-FPGA) is another type of FPGAs based on AS technology. ASs are programmable conductive bridges electrically formed between two metals grown by the electrochemical phenomenon. ASs have a Ru-Polymer solid electrolyte (PSE)-Cu sandwich structure. As the formation or annihilation of a Cu ion bridge causes a low or high resistance states corresponding to each digital state, it is classified as resistive random access memory (RRAM).

Historically, Eigler *et al.* [2] manipulated Xe atoms by using a scanning tunneling microscope and introduced the concept of the "atomic switch." Li and Tao [3] demonstrated metal bridge deposition and dissolution in an electrolyte, showing the quantized conductance. Terabe *et al.* [4] also succeeded to control the atomic bridge at the crossing point between the metal electrode and solid electrolyte. The features of ASs (i.e., small nanometer-scale order size, nonvolatility, high ON/OFF resistance ratio) make the devices attractive. ASs have been successfully applied in nonvolatile memories and FPGAs for their configuration memory cells and routing switches [5], given the compatibility with the fabrication process for complementary metal–oxide–semiconductor (CMOS). ASs are already known in such nonvolatile memory applications as conductive bridge random access memory (CBRAM) [6].

Such back-end-of-the-line (BEOL) technologies, along with conventional CMOS technology should also withstand harsh space environments. Highly integrated BEOL and CMOS processes show complex characteristics in terms of radiation effects, and thus we cannot easily separate the cause of errors. Although monoenergetic heavy ions accelerated from a cyclotron are widely accepted and utilized to evaluate radiation effects in semiconductor devices, pulsed laser irradiation is also an effective way to analyze spatial characteristics of the devices, even in submicrometer-scale semiconductor technology node processes. In particular, for BEOL technology, laser testing will help us to isolate faults between CMOS and ASs because a pulsed laser cannot pass through metal layers.

Previous studies have reported gamma-ray tolerance for Ag/GeS_2/W-based CBRAM [7], and total dose effect [total ionizing dose (TID)] and displacement dose (DD) damage on Al/Ag/Ag-$Ge_{30}Se_{70}$/Ni-based CBRAM [8]. These results suggest CBRAM has the intrinsic several hundreds krad to10 Mrad TID tolerance, though these element compositions are different from ASs. Other studies have reported that an Ag-based CBRAM exhibits single-event upsets (SEUs) due to upsets of the access transistors [9] and that the Ag-based standalone memory chip is vulnerable to bit upsets during dynamic write/read tests [10]. These results imply that CBRAM has intrinsic tolerance to radiation in terms of both TID and SEEs,

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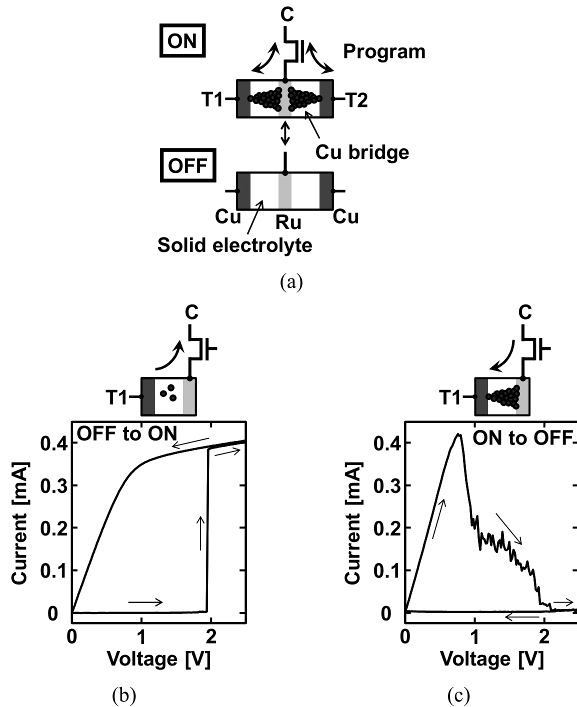


Fig. 1. (a) Schematic of CAS that show ON and OFF states. (b) and (c) I–V characteristics for set and reset operations of ASs.

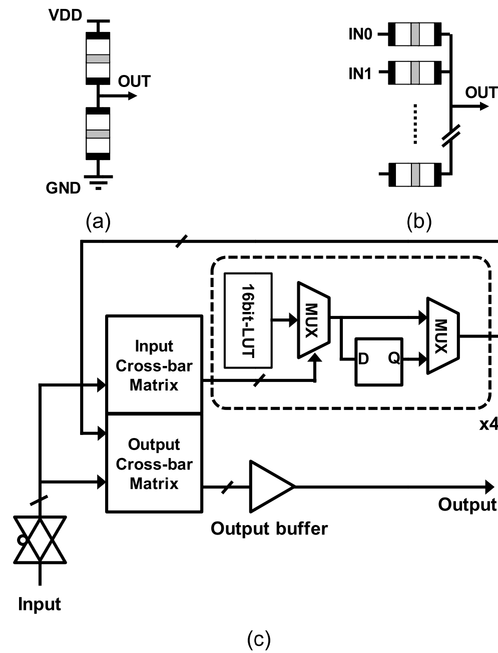


Fig. 2. (a) Illustration of the CAS-based memory cell used in LUT. (b) Illustration of the CAS-based routing MUX [11], [12]. (c) Schematic of a unit logic tile (details are described in [13]).

and circuit topology may also affect its radiation tolerance. In ASs of FPGA applications, unlike memory applications, ASs are always biased and suffer from voltage stress in routing switches. Therefore, the form of FPGAs is a reasonable way to evaluate these phenomena.

In this work, we evaluate AS-FPGAs in terms of SEUs and single-event transients (SETs). Heavy-ion and pulsed laser irradiation were conducted to investigate these SEEs. The paper is organized as follows. Section II gives the AS-FPGA device specifications. Section III describes the conditions of the heavy-ion and pulsed laser experiments including sample chip preparation. Section IV presents experimental results focusing on SET generation in the test chip. Section V provides the SET mitigation outlook combined with the AS-FPGA application and discusses the circuit and device simulation results.

II. AS-FPGA

The ASs are utilized in the FPGA as a complimentary AS (CAS), in which the ASs are connected in series with the opposite direction [11], [12].

Fig. 1(a) shows schematic images of CAS which show ON and OFF states. The logic signal passes through between T1 and T2 of CAS in the crossbar matrix during the logic operation. Both ASs are programmed to be in the ON or OFF state by sequentially applying a voltage between terminals T1 and C, and T2 and C.

When a positive voltage is applied to T1 (or the Cu electrode) as shown in Fig. 1(b), Cu is ionized and precipitated at the Ru electrode, and then a Cu metal bridge is formed between the Cu and Ru electrodes. The conductance of AS changes to high (i.e., the ON state). This is called the set operation. The current during the programming is regulated by the n-type transistor connected to the middle node of CAS so as to control the on conductance.

When a positive voltage is applied to C (or the Ru electrode) as shown in Fig. 1(c), the Cu metal bridge is broken and dissolved into the solid electrolyte and the switch turns off. This is called the reset operation. The programming time for the set and reset operations is 1 and 0.2 μs, respectively. Moreover, a certain amount of current (0.4 mA in this case) is required to set or reset the ASs as shown in Fig. 1. The other AS in CAS is also programmed via terminals C and T2. The ON resistance of ASs is controlled to be from 0.5 to 5 kΩ by varying the set current. In this SEE experiment, the ON resistance is programmed to be 1 kΩ.

Fig. 2(a)–(c) shows the CAS-based memory cell, the CAS-based routing selector, and the unit logic tile, respectively. Each logic tile has four sets of D-type flip-flops (FFs), CAS-based four-input lookup tables (LUTs), and multiplexers (MUXs). It also has the crossbar matrix for interlogic tile connection. The logic tiles are interconnected through this crossbar matrix. The CASs are used in LUTs, MUXs, and the cross-bar matrix in the logic tile of AS-FPGA. The AS-FPGA chip is 5 mm $\times$ 5 mm in size, composed of 44 $\times$ 48 programmable logic tiles and a 4 $\times$ 48 RAM block array. The chip contains about 12.7 million ASs.

III. Experimental Setup

A. Sample Preparation

Two types of test vehicles were fabricated in the 40-nm node bulk CMOS process as the prototype of the AS-FPGA to evaluate AS immunity against irradiation. One is AS-FPGA, in which ASs are integrated with CMOS and programmed to connect lines in the cross-bar matrix and LUTs. The other is

TABLE I
LIST OF SAMPLES

Samples	D-FF	Configured circuit (8 chains in parallel)
AS-FPGA w/o D-FF	No	I/O logic — buffers — I/O logic
AS-FPGA w/ D-FF	Yes	I/O logic — D Q (CLK) — buffers — D Q (CLK) — I/O logic
Hard-via-FPGA	Yes	

TABLE II
HEAVY-ION TEST CONDITIONS

Ion	Net Energy [MeV]	LET at Si surface [MeV/(mg/cm^2)]	Range in Si [μm]
Xe	398	68.9	35.0
	296	67.2	28.5
Kr	289	40.3	37.3
	197	40.8	27.6

a hard-wired gate array (hereinafter called “Hard-via-FPGA”) in which the ASs are not integrated and the ASs programmed to be in the ON-state in AS-FPGA are replaced by a metal via the back-end process. Each side of the chip was exposed to the surface to introduce ions and a pulsed laser. Two kinds of chains with or without D-FFs (hereinafter called “AS FPGA without D-FF”) were programmed to evaluate SETs. The “w/D-FF” chains were subjected to compare AS-FPGA and Hard-via-FPGA so as to evaluate degradation and/or state change of ASs.

Table I shows schematic diagrams of the buffer chain circuit configured in each FPGA, which was composed of 132 or 264 stages of unit buffer blocks connected in series in each chain, and eight chains were connected in parallel. The chains were configured over 1584 (48 × 33) logic tiles. Other logic tiles and RAM blocks were also monitored for the state change of ASs. In a unit logic tile, 360 of 5544 ASs were programmed to be in the ON state, with the other ASs in the OFF state. The AS in the chips were programmed for SETs evaluation circuits and validated before and after irradiation by the large scale integrated circuit tester. The input–output (I/O) logic is composed of I/O transistors and voltage level shift circuitry, which translates I/O signal voltage and internal logic signal voltage; in this case, 2.2 and 1.6 V. All experiments were conducted at room temperature.

B. Heavy-Ion Irradiation

The radiation tolerance of AS-FPGAs was evaluated by using the Takasaki Ion Accelerators for Advanced Radiation Application (TIARA) at the National Institutes for Quantum and Radiological Science and Technology (QST). A cocktail-heavy-ion beam of Xe and Kr was used for the evaluation. Table II lists the irradiated ions and related information. All irradiations were performed at normal incidence.

C. Pulsed Laser Irradiation

PULSCAN [14] is the test system for pulsed laser irradiation and was utilized for the experiment. The wavelength and pulse duration are 1064 nm and 30 ps, respectively. Thus, single-photon laser absorption was used for evaluation to trigger SEUs and SETs in the CMOS layer. The laser was irradiated via the backside of the chip which is composed of a Si substrate and does not affect ASs in metal layers. The pulsed laser shows a 2-D Gaussian intensity distribution in the focal plane, and its full-width at half-maximum (FWHM) of intensity is 4.2 μm with a 20× objective lens. Although that is relatively larger than the transistor size in this fabrication process, it is good enough to find weak points in the logic tile (about 85-μm square). The test conditions and other aspects of the setup are consistent with the heavy-ion experiments.

IV. RESULTS AND DISCUSSIONS

A. Heavy-Ion Irradiation

1) State Change of ASs: No state changing of ASs was observed up to 68.9 MeV/(mg/cm^2) with 10^7 particle/cm^2 of ion fluences, with respect to all samples. About 1909 particles were expected to hit somewhere in the ASs on FPGA, assuming that the cell area (conductive bridge area) of ASs was 1.5×10^{-11} cm^2. The cross section for ON-to-OFF state transition is estimated to be up to 1.8×10^{-13} cm^2. Although the power supply current was slightly increased and decreased repeatedly when ions were irradiated, there was no latch-up event or sudden increase in the current. Furthermore, no permanent degradation of power supply current was found after irradiation.

Circuits on the FPGA could be normally written and erased even after irradiation. Despite the numerous SETs (>300 SETs as mentioned later) that occurred in the experiment, the configured circuit was never changed throughout the experiment. This offered strong evidence of the immunity to the state change of ASs.

2) SETs and SEUs in D-FF: SETs were observed, however, during both heavy-ion and pulsed laser irradiation. Fig. 3(a) shows a box-and-whisker plot and histogram of the SET cross section with AS-FPGA w/o D-FF. In Fig. 3(a), the boxes extend from the lower to upper quartile values of the data in what is called the interquartile range (IQR) and the red lines indicate the median. The whiskers extending from each box show the range of the data. The outlier (defined as the point exceeding ±1.5 times the IQR from the median) is plotted as the “+” mark. Each SET cross section (σ_{SET} [cm^2/logic tile]) is calculated by the following formula:

$$\sigma_{\mathrm{SET}} = \frac{1}{(\text{SET intervals}) \times (\text{flux}) \times (\text{\# of logic tiles})} \quad (1)$$

where (SET intervals), (flux), and (# of logic tiles) are the intervals of each SET in second, the averaged flux in p/cm^2/s, and the total logic tiles used in the configured circuit, respectively.

As shown in Fig. 3(a), the SET cross sections of AS-FPGA without D-FF exhibit linear energy transfer (LET) dependence and clearly different SET distributions. The distributions of SETs suggest that they were caused by heavy ion interactions, which are random processes. Since AS-FPGA w/ D-FF and Hard-via-FPGA chips that include D-FFs at both ends of the

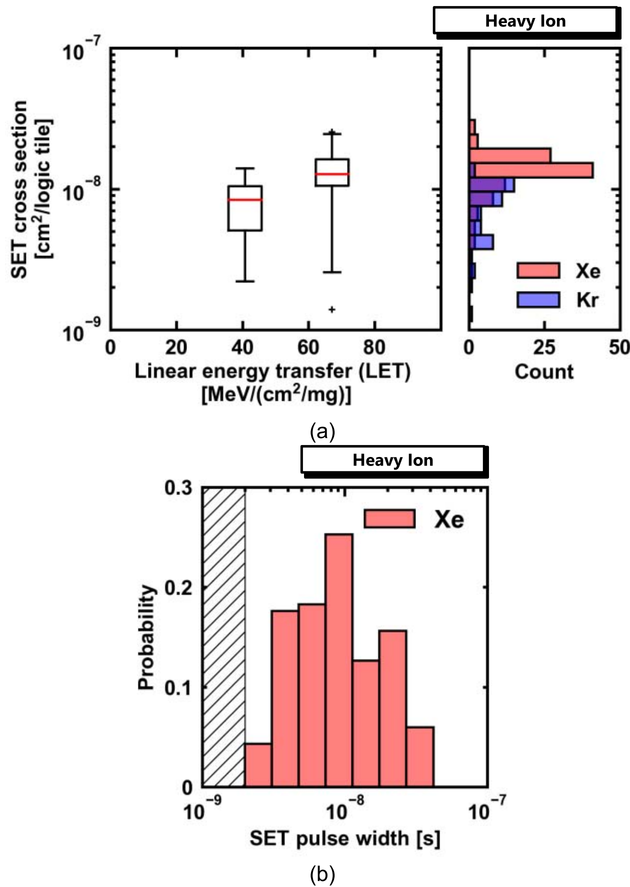


Fig. 3. (a) Box-and-whisker plot and histogram of SET cross section in AS-FPGA w/o D-FF. (b) Histogram of SET pulsewidth distributions acquired in Xe irradiation with AS-FPGA w/o D-FF. Shaded area: unreliable region due to less sampling resolution.

buffer chain are clocked at a certain frequency (1 to 100 MHz), SET acquisition probabilities become higher as the frequency increases. Both chips had no significant difference with respect to the SET cross section at each operating frequency. Thus, it is concluded that the CMOS layer causes the SETs and that ASs do not cause any SET noise when the ions hit.

Fig. 3(b) shows the distributions of SET pulsewidth. The SET pulsewidth in AS-FPGA without d-type flip-flop was randomly distributed from nanoseconds to a few tens of nanoseconds regardless of the operating frequency. Previous research related to these technology nodes has reported that the SET pulsewidth is a few hundreds of picoseconds [15], [16]. The SET pulsewidth acquired in this experiment showed one to two orders of magnitude greater than that of the previous study. This prolonged SET pulse is discussed in the following sections by using the pulsed laser and simulation results. From the SETs cross section, ASs would not be considered a direct cause of SETs. The pulsed laser test was conducted to reveal the source of SETs in the logic tile.

B. Pulsed Laser Irradiation

Fig. 4 shows the results of the pulsed laser irradiation. The blue area in the unit logic tile (gray square) was scanned by a pulsed laser and yellow colored dots represent the points where SET occurred. SETs were mainly captured from

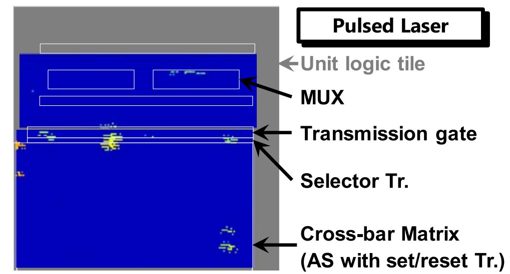


Fig. 4. Example result of pulsed laser irradiation test at 9000 pJ. Blue areas are scanned by laser, and yellow colored dots represent the points where SET occurred. Gray square: area of the unit logic tile. White-lined squares: functional modules in the logic tile.

MUX and the cross-bar matrix, as well as modules composed of unhardened CMOS logic such as transmission gates and selector transistors. Only set/reset transistors that are I/O high voltage transistors and associated with ASs are used in the cross-bar matrix.

The pulsed laser was manipulated in 0.5-μm steps; hence, each point represents 0.25 μm^2 in the cross section. As laser FWHM is 4.2 μm, SETs were captured like insular shape, distorted along the scanning direction. In this case, it was a horizontal meander pattern. The locations where SETs were captured are consistent with the configured module in the logic tile. The cross sections of SETs in pulsed laser testing (distributed about 10^{-8} to 10^{-6} cm^2/logic tile) were varied with laser energy and were roughly consistent with the heavy-ion test. All SETs that occurred in pulsed laser irradiation should come from the CMOS layer because the laser could not reach the ASs located between the metal layer.

The SET pulsewidth captured in the laser test differed in irradiated places in the buffer chains. The SET pulsewidth observed in a short logic tile length (less than ten logic tiles to the end of the buffer chain) is distributed from subnanoseconds to 5 ns. In general, the I/O logic bandwidth of this process design should be around a few hundred megahertz, and the subnanosecond pulse would be normally filtered by I/O logic. The set/reset transistors with ASs may be responsible for the unexpectedly prolonged SETs.

V. SETs Mitigation Outlook

Fig. 5 shows the simulated SET pulse that was generated in the n-type transistor connected to CAS [Fig. 1(a)] in the crossbar matrix of the logic tile. In the simulation, the switch was inserted to generate SET in the transistor [17]. For 100 to 1000 ps, the switch was turned on to generate a transient noise and then the output signal of the logic tile was monitored. The transient noise was observed in the output when the duration of SET is more than 200 ps and affected the output signal of the logic tile as shown in Fig. 5.

In the previous discussion, unhardened CMOS and n-type transistors with ASs were revealed to cause the SETs. In order to mitigate SETs, some measures are required for the AS's peripheral, in which high-voltage transistors are utilized. Fig. 6 shows our proposed alternative circuits, and SPICE and semiconductor technology computer-aided design (TCAD) simulation were conducted to check those

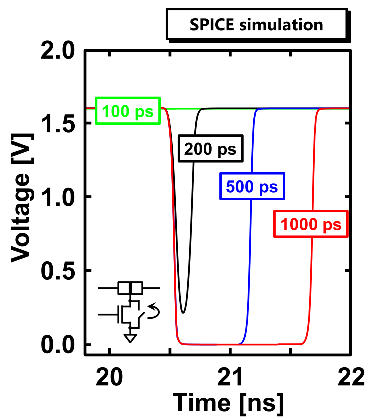


Fig. 5. SPICE simulation results. The switch inserted in parallel with the set/reset transistor of AS was switched on for 100–1000 ps. The logic tile output voltage is plotted as a function of time.

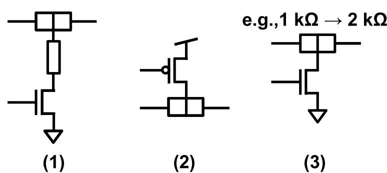


Fig. 6. SET mitigation examples for AS crossbar circuits. (1) Inserting the series resistance. (2) Replacing n-type transistor with p-type. (3) Increasing the resistance of ASs.

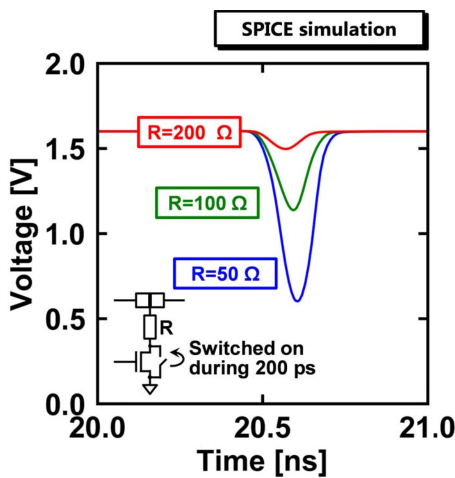
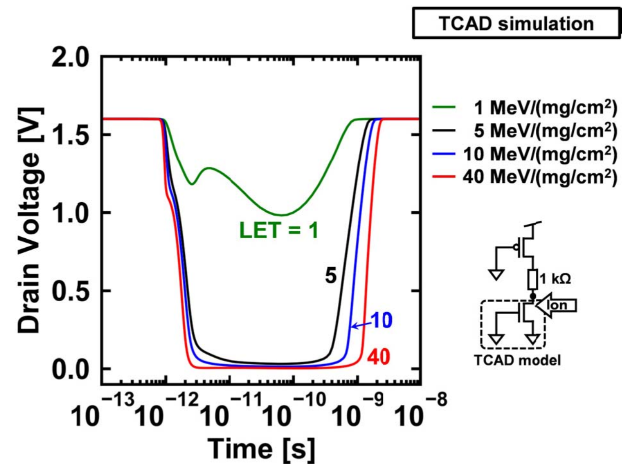


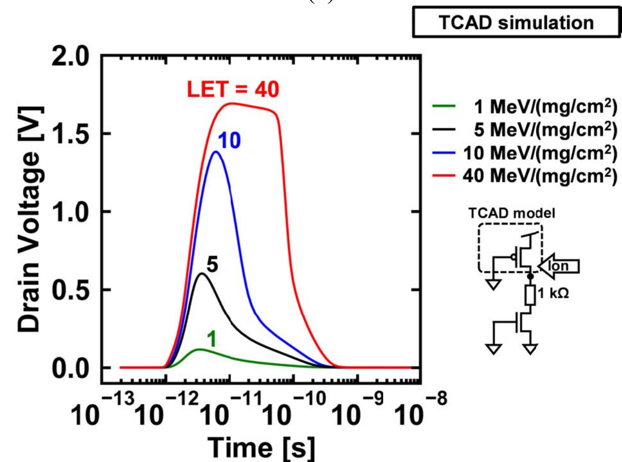
Fig. 7. SPICE simulation results of series resistance insertion. Transient noise became smaller when larger series resistance was inserted.

circuits for mitigating SETs as follows: 1) inserting series resistance to the set/reset transistor, 2) replacing the n-type transistor with the p-type, or 3) increasing the on resistance of ASs. These methods reduce the amplitude and/or duration of the SET pulse. Fig. 7 shows the SPICE results which suggest that a smaller drop in transient noise of the logic tile occurs in output. Although a logic speed penalty should be considered, increasing the resistance of ASs gives the same effect. It should be noted that AS-FPGA can control SET tolerance on the field, given the tunable resistance of ASs by programming.

Fig. 8 presents the results of 3-D TCAD mixed-mode simulation (combining TCAD and SPICE simulation) using the Hyper Environment for Exploration of Semiconductor Simulation (HyENEXSS) simulator [18]. The TCAD transistor



(a)



(b)

Fig. 8. TCAD mixed-mode simulation results of n-type and p-type transistors. (a) and (b) Simulation results of drain output voltage when 1, 5, 10, 40 MeV/(mg/cm^2) ions hit the drain in n-type and p-type transistors, respectively.

profile was based on [19] and calibrated by dc parameters. The 1-kΩ resistance used to imitate connected ASs and the transistor defined in the SPICE model were connected as shown in Fig. 8(a) and (b). The TCAD MOSFET for the simulation was defined as being about $0.1 \times 1 \times 1.5\ \mu\text{m}^3$. The spatial and temporal profiles of the electron–hole (e-h) pair were chosen as a 50-nm constant radius with 1-nm characteristic 1/e decay and Gaussian 1-ps characteristic time, respectively, to simulate the charge deposition of the incident ion. The track was extended to 1 μm below the drain electrode along the z-axis (normal to the surface of the MOSFET).

The SETs of drain output were plotted in Fig. 8(a) and (b) as a function of time. It is clear that the p-type set/reset transistor considerably reduces the SET response. In Fig. 8(a), the 40 MeV/(mg/cm^2) ion that hits in nMOS generates transient noise lasting 1 ns or more. The distribution of SET pulsewidth shown in Fig. 3(b) can be reasonably explained by considering the pulse-broadening effects. It was also confirmed that the transient response for 200 ps of the turn-on time shown in Fig. 8 roughly corresponded to a LET between 1 and 5 MeV/(mg/cm^2) in comparison with the TCAD simulations.

VI. Conclusion

ASs exhibited immunity to a state change up to 68.9 MeV/(mg/cm^2), irrespective of the cell states. However, the set/reset transistor was identified as being responsible for causing the unexpectedly prolonged SETs. The possible techniques were discussed with simulations to utilize ASs in space applications in terms of SEEs. The TID response of these technologies must be characterized for further understanding of the radiation response.

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